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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/791,759	03/04/2004	Douglas J. Bonser	50432-645	5274

7590 10/14/2005

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EXAMINER	
TRAN, LONG K	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 10/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H:A

Office Action Summary	Application No.	Applicant(s)	
	10/791,759	BONSER ET AL.	
	Examiner	Art Unit	
	Long K. Tran	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/4/04; 6/21/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. This office acknowledges of the following items from the Applicant:

Information Disclosure Statements (IDS) filed on March 04, 2004 and on June 21,2005.

The references cited on the PTO -1449 form have been considered.

Specification

2. The specification has been checked to the extent necessary to determine the presence of possible minor errors. However, Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claim **1** is rejected under 35 U.S.C. 102(b) as being anticipated by Meyer (US Patent No. 5,665,633).

5. Regarding claim **1**, Meyer discloses a method of fabricating a semiconductor device the method comprising:

forming a nitride polish stop Layer 44 (fig. 4; column 3, lines 41 – 43), at a thickness no greater, than 400 ANGSTROMS over a semiconductor substrate (note that

"*Layers 42 and 44 have substantially uniform thicknesses in a range of about 100-500 angstroms each. The combined thickness of layers 42 and 44 typically does not exceed about 1000 angstroms and is usually no more than 500 angstroms*" (column 3, lines 45 – 49)), over a semiconductor substrate;

forming an opening in the nitride polish stop layer 44 and a trench 52/54 (fig. 5; column 3, lines 50 – 53) in the substrate;

filling the trench 52/54 with insulating material 62 (fig. 6; column 4, lines 6 – 15) forming an overburden on the nitride polish stop layer 44; and

polishing to form an upper planar surface stopping on the nitric polish stop layer, thereby forming a shallow trench isolation region 72/74 (fig. 7; column 4, lines 16 – 31).

Regarding claim **4**, Meyer discloses comprising forming a pad oxide layer 42 (fig. 4; column 3, line 43 – 45) on an upper surface of the semiconductor substrate 10, and forming the nitride polish stop layer 44 on the pad oxide layer 42.

Regarding claim **5**, Meyer discloses ion implanting impurities through the nitride polish stop/nitride gate dielectric layer 102 (fig. 11) to form impurity regions 1162/1164/1182/1184 (fig. 11) in the semiconductor substrate 10 adjacent the shallow trench isolation region 62 (fig. 11; column 4, lines 1 – 3 and lines 10 – 19).

Regarding claim **6**, Meyer discloses removing the nitride polish stop layer 44 (column 4, lines 60 – 61);

forming a gate oxide layer 102 (fig. 9; column 4, lines 66 – 67 and column 5, lines 1 – 3) on the semiconductor substrate after removing the nitride polish stop layer 44; and

forming a gate electrode 112/116/118 (fig. 11; column 5, lines 3 – 5) on the gate oxide layer 102.

Regarding claim **7**, Meyer discloses etching to remove part of an upper surface of the insulating material filling the trench so that the upper surface of the insulating material is substantially coplanar with the upper surface of the semiconductor substrate before removing the nitride polish stop layer (abstract; column 3, lines 1 – 35 and column 4, lines 16 – 20).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims **2** and **3** are rejected under 35 U.S.C. 103(a) as being unpatentable over Meyer (US Patent No. 5,665,633).

Regarding claim **2**, Meyer discloses the claimed invention of claim 1 and further teaches forming nitride polish stop layer at a thickness of 100 angstroms to 500 angstroms (column 3, lines 45 – 49). Meyer fails to teach the nitride polish stop layer at thickness 50 angstroms to about 100 angstroms as the instant claim.

However, it would have been obvious to one of ordinary skill in the art of making semiconductor devices to form the workable or optimal ranges for the nitride polish stop layer having modified thickness of 50 angstroms to about 100 angstroms through routine experimentation and optimization to obtain optimal device performance.

Regarding claim **3**, Meyer discloses the claimed invention of claim 1 and further shows "Insulating layer 62 to remove portions of it overlying the polish stop layer 44". Meyer does not explicitly shows polishing to form the upper planar surface while removing no more than 20 angstroms of the nitride polish stop layer 44 as the instant claim.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust parameters of the polishing process to remove part of the polish stop layer no more than 20 angstroms as claimed to insure all insulating material of layer 62 that overlying the polish stop layer has been removed through routine experimentation and optimization to obtain optimal device performance.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Liu et al. (US Patent No. 6,248,641) and kepler et al. (US Patent No. 6,599,810) disclose a method of fabricating a semiconductor device similar to that of Meyer (US Patent No. 5,665,633).

9. A shortened statutory period for response to this action is set to expire e (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02 (b)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long K. Tran whose telephone number is 571-272-1797. The examiner can normally be reached on Mon-Thu.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LKT

October 11, 2005